WHAT IS CLAIMED IS:

1. A circuit comprising:

a plurality of outputs to provide a sequence of clock signals which together comprise a multistage clock; and

a delay adjustment input to adjust the timing of the clock signals for at least one of the outputs relative to the clock signals at another of the outputs.

2. The circuit of claim 1, wherein the delay adjustment input adjusts the timing of the clock signal at said one output and at all of the outputs that follow said one output in the multistage clock, wherein said adjustments are relative to the output that precedes said one output in the multistage clock.

3. The circuit of claim 2, wherein the circuit has a plurality of said delay adjustment inputs.

4. A circuit comprising:

a clock input to receive a clock input signal;

a plurality of clock outputs to each provide a delayed version of the clock input signal, wherein the amount of delay in the signal at each of the clock outputs differs from the amount of delay in the signal at the other clock outputs by approximately a multiple of a time *t*; and

a delay adjustment block to vary the difference in the amount of delay in the signal at one of the clock outputs compared to the signal at another of the clock outputs.

5. The circuit of claim 4, wherein the delay adjustment block has an input to digitally control the variation in the amount of delay.

6. The circuit of claim 5, wherein the circuit has a plurality of said delay adjustment blocks, wherein the clock outputs have a sequential order, and wherein each of the delay adjustment blocks varies the delay between a clock output and all of the clock outputs that follow that output in the sequential order.

7. The circuit of claim 6, wherein the time *t* is approximately the delay of an inverter with a fanout of 2.

8. A circuit comprising:

a clock input;

a plurality of clock outputs each connected by a path to the clock input;

a plurality of first delay blocks each of which is part of a single path from the clock input to one of the clock outputs;

a plurality of second delay blocks each of which is part of one of said paths from the clock input to a clock output through one of the first delay blocks and is part of another path from the clock input to another clock output through another first delay block; and

an delay adjustment block connected to an output of one of the second delay blocks.

9. The circuit of claim 8, wherein said first delay blocks and second delay blocks each comprise a pair of inverters connected serially.

10. The circuit of claim 9, wherein the delay adjustment block comprises a pair of transistors connected serially.

11. The circuit of claim 8, wherein the delay adjustment block is a digital variable delay block.

12. A method of providing a plurality of delayed clock signals, the method comprising:

receiving a clock signal at a point in a circuit;

delaying the received clock signal using a first pair of inverters to provide a first clock output signal;

delaying the received clock signal using a second pair of inverters to provide a second clock output signal that is delayed by approximately a time *t* from the first clock output signal;

delaying the received clock signal using a first delay block to provide a first internal clock signal that is delayed by approximately time *2t* from the received clock signal; and

delaying the first internal clock signal using a third pair of inverters to provide a third clock output signal that is delayed by approximately time *t* from the second clock output signal.

13. The method of claim 12, wherein the first delay block comprises a pair of inverters.

14. The method of claim 13, wherein providing a first internal clock signal includes:

receiving a first enable input signal; and

delaying the first internal clock signal by creating a contention current.

15. The method of claim 14, wherein creating the contention current comprises turning on a transistor to create a path to ground for the first internal clock signal.

16. The method of claim 12, further comprising:

delaying the first internal clock signal using a fourth pair of inverters to provide a fourth clock output signal that is delayed by approximately time *t* from the third clock output signal;

delaying the first internal clock signal using a second delay block to provide a second internal clock signal that is delayed by approximately time *2t* from the first internal clock signal;

delaying the second internal clock signal using a fifth pair of inverters to provide a fifth clock output signal that is delayed by approximately time *t* from the fourth clock output signal; and

delaying the second internal clock signal using a sixth pair of inverters to provide a sixth clock output signal that is delayed by approximately time *t* from the fifth clock output signal.

17. The method of claim 16, wherein providing a second internal clock signal includes:

receiving a second enable input signal; and

delaying the second internal clock signal by creating a contention current.

18. The method of claim 17, wherein the time *t* is approximately equal to the delay of an inverter with a fanout of 2.

19. A circuit comprising:

a clock input;

a first chain of two inverters having an input connected to said clock input and having an output connected to a first clock output;

a second chain of two inverters having an input connected to said clock input and having an output connected to a second clock output;

a third chain of two inverters having an input connected to said clock input and having an output; and

a fourth chain of two inverters having an input connected to the output of the third chain of inverters and having an output connected to a third clock output.

20. The circuit of claim 19, further comprising:

a first transistor connected to the output of the third chain of inverters and having a gate connected to a first enable input; and

a second transistor connected to the first transistor and to ground.

21. The circuit of claim 20, wherein the circuit further comprises:

a fifth chain of two inverters having an input connected to the output of the third chain of inverters and having an output connected to a fourth clock output;

a sixth chain of two inverters having an input connected to output of the third chain of inverters and having an output; and

a seventh chain of two inverters having an input connected to the output of the sixth chain of inverters and having an output connected to a fifth clock output.

22. The circuit of claim 21, wherein the second transistor has a gate that is connected to a point between the inverters in the sixth chain of inverters.

23. The circuit of claim 22, wherein the circuit further comprises:

an eighth chain of two inverters having an input connected to the output of the sixth chain of inverters and having an output connected to a sixth clock output;

a ninth chain of two inverters having an input connected to output of the sixth chain of inverters and having an output;

a tenth chain of two inverters having an input connected to the output of the ninth chain of inverters and having an output connected to a seventh clock output; and

a third transistor connected to the output of the ninth chain of inverters and having a gate connected to a second enable input.

24. A method of adjusting the delay of a clock signal in a multistage clock, the method comprising:

determining that the delay between one stage of a multistage clock and the following stage of the multistage clock is too large; and

setting a first storage element which will later cause the input of a clock adjustment signal to a clock delay circuit and thereby reduce the delay between said one stage of the multistage clock and said following stage.

25. The method of claim 24, wherein the method further comprises:

determining that the delay between a third stage of the multistage clock and a fourth stage of the multistage clock is too large; and

setting a second storage element which value will later cause the input of a second clock adjustment signal to the clock delay circuit and thereby reduce the delay between said third stage and said fourth stage.

26. The method of claim 25, wherein setting the first storage element reduces the delay between said one stage and all following stages.

27. The method of claim 24, wherein the delay is reduced by creating a contention current.